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F rmati n f thin semic nductor layers by low-energy plasma enhanced chemical vapor deposition and semiconductor heterostructure devices

[0001] The present invention concerns the formation of thin semiconductor layers, in particular silicon-germanium layers, by means of a plasma enhanced chemical vapor deposition process, and semiconductor heterostructure devices made by means of the plasma enhanced chemical vapor deposition process.

Background of the invention

[0002] New materials and material compositions are being employed in industry in order to improve semiconductor devices such as transistors, for example. This allows one to improve the processing speed and performance of integrated circuits (ICs). A typical example is the deployment of a thin strained silicon film on top of a relaxed Silicon-Germanium (SiGe) buffer layer, on a Silicon (Si) substrate.

[0003] A conventional approach of using relaxed graded SiGe layers as buffers is now described. The concept of graded SiGe buffer layers was invented in 1991 by Fitzgerald et al. The results of their work are described in F.A. Fitzgerald, Y.-H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y.-J Mii, and B. E. Weir, Appl. Phys. Lett., Vol. 58, p. 811, 1991. Such buffer layers are used as virtual substrates (VS) for applications in the area of high-speed electronics by means of metal-oxide semiconductor field-effect transistors (MOSFETs) and modulation-doped field-effect transistors (MODFETs) based on strained Si or $Si_{1-x}Ge_x$ ($0 < x \leq 1$). The active layers (e.g., Si) on top of a VS are strained because the VS has a lattice parameter intermediate between that of Si and Ge.

[0004] In the graded buffer approach, the Ge concentration x in a $Si_{1-x}Ge_x$ alloy is raised in a linear or step-wise fashion from zero up to some final value x_f.

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In this way, dislocations are distributed in a larger volume compared to a SiGe film with constant composition, where they reside basically at the interface. As a result, threading dislocation (TD) arms become more mobile, long misfit segments are formed (ideally across the whole wafer) and the density of TDs piercing the active layers of devices, and spoiling their performance, is reduced.

[0005] To date, the highest low-temperature electron and hole mobilities in strained Si channels were reported in the following two papers: K. Ismail, M. Arafa, K.L. Saenger, J.O. Chu, and B.S. Meyerson, in Appl. Phys. Lett., Vol. 66, p. 1077, 1995; P. Weitz, R.J. Haug, K. Von Klitzing, and F. Schäffler, in Surf. Sci. 361/362, p. 542, 1996; and in strained Ge channels by H. von Känel, M. Kummer, G. Isella, E. Müller, and T. Hackbarth, in Appl. Phys. Lett., Vol. 80, p. 2922, 2002. This has been achieved using VS based on Fitzgerald's concept.

[0006] Conventional VS are, however, typically several microns thick because the grading rates have to be kept low (typically around 10%/µm) to assure low TD densities. Such VS are therefore very time consuming to fabricate with conventional growth techniques.

[0007] There does, however, exist a fast deposition process, called low-energy plasma-enhanced chemical vapor deposition (LEPECVD) by means of which time and material consumption has been minimized. The basic process, applied only to Si and SiGe films of a "quality sufficient for epitaxy", is described and claimed in the US patent with patent number US 6,454,855 B1, and in a pending PCT application published as WO 98/58099.

[0008] For the application of LEPECVD to p-MODFETs, a European patent application was filed on 22 November 2001. Application number 01127834.8 was assigned. Subsequently, a PCT patent application was filed on 5 September 2002 and the international application number PCT/EP 02/09922 was assigned. In the context of these applications 01127834.8 and PCT/EP 02/09922, the LEPECVD is used to grow thick graded relaxed SiGe layers. It is a disadvantage of thick graded SiGe buffer layers, that their thermal conductivity is relatively low. When using a substrate with such a thick SiGe buffer layer, heat dissipation might be a

problem in particular in highly integrated circuits. If one uses a substrate with a thick SiGe buffer layer, the integration of Si circuits is difficult, since there are substantial differences in heights (large step heights) between the buffer and those areas where the buffer has been removed by means of etching. Photolithography on such a structured surface is difficult due to focusing problems, for instance.

[0009] Even though VS based on thick graded relaxed buffer layers can now be economically grown, e.g., by LEPECVD, the thick VS concept implies major disadvantages, such as

- poor thermal conductivity, leading to problems with heat dissipation for SiGe devices, as mentioned above,
- large surface roughness due to cross-hatch, requiring chemical mechanical polishing
- problems with integration because of large step heights due to large SiGe layer thickness, as mentioned above.

[0010] In the following, thin relaxed buffer layers serving as VS are addressed. In the past few years many attempts have been made to overcome the shortcomings of thick conventional graded buffers, aiming at a substantial reduction of buffer layer thickness to the range of 100 – 500 nm. In almost all cases these efforts have been carried out by means of solid source molecular beam epitaxy (MBE), which is not a suitable technique for large scale production. One notable exception is the work by K. K. Linder et al., who used gas-source molecular beam epitaxy and ultrahigh vacuum chemical vapor deposition. For details please refer to K. K. Linder et al., Appl. Phys. Lett., Vol. 70, p. 3224, 1997. These processes are, however, extremely slow, of the order of a mono-layer per minute or less, at the low substrate temperatures required.

[0011] The most serious disadvantage of MBE is the limited capacity of the evaporation crucibles. This is a disadvantage in particular when growing SiGe-buffer layers having a thickness of up to 500 nm. MBE is thus not well suited for industrial production of devices comprising SiGe layers.

[0012] CVD processes in general, are not deemed to be suitable for deposition at low substrate temperatures even for VS thinner than ~ 500 nm. In the "Handbook of thin-film deposition processes and techniques", ed. Klaus. K. Schuegraf, Noyes Publications, New Jersey, USA, 1988, ISBN: 0-8155-1153-1, p. 26 through 79, there is an overview article by M. L. Hammond addressing Si epitaxy using CVD. It is clear from this article that there is an exponential decrease of the growth rate as the substrate temperature decreases. Estimates based on figures from various publications indicate that Si would grow at a rate between 0.01 nm/min and 0.0001 nm/min if using a CVD process at about 400°C. A SiGe alloy layer would probably grow at a rate that is certainly below 1nm/min (0.0166 nm/s) if one were to use a CVD process at about 400°C.

[0013] One concept that was investigated is the deposition of a low temperature Si buffer before SiGe growth. The idea of this so-called low-temperature silicon (LT-Si) buffer was introduced by H. Chen et al., J. Appl. Phys., Vol. 79, p. 1167, 1995. Chen proposed a two-step growth process. It is based on the following premise: Silicon epitaxially grown at low substrate temperatures (typically of the order of 400°C) contains a high concentration of point defects. These point defects may diffuse to the interface during subsequent SiGe growth at higher substrate temperature, and promote the nucleation of dislocation loops. Relaxation of the SiGe film therefore no longer requires formation of dislocation half-loops at the surface. Since the half-loops are associated always with two TDs, reducing their density should also reduce the density of TDs.

[0014] It is a disadvantage of this two-step growth process that it appears to fail at Ge concentrations x above ~ 30%. It is, however, applicable to higher x if layers are grown in more than one step (cf. C.S. Peng et al., Appl. Phys. Lett., Vol. 72, p. 3160, 1998). Such a procedure is evidently time consuming.

[0015] Another two-step growth process starts with the epitaxial growth of SiGe at ultra-low temperatures. According to this concept, advocated by E. Kasper et al. in Thin Solid Films, Vol. 336, p. 319, 1998, it is the SiGe film itself which is grown in a first step at very low temperatures of the order of 200° C by

MBE. In a second step, the VS is completed by growing the film to its final thickness at a higher temperature (cf. M. Bauer et al. in Thin Solid Films Vol. 369, p. 152, 2000). The idea here is that point defects in the film should help dislocations with opposite Burgers vector to annihilate, because of dislocation climb. Furthermore, as in the case of LT-Si, condensation of point defects can result in the formation of dislocation loops inside the SiGe layer, avoiding dislocation nucleation from surface sites. It is a disadvantage of the concept advocated by E. Kasper et al., that it requires MBE.

[0016] Another approach is the post SiGe growth hydrogen ion implantation or H-cleaning plus annealing. In this approach, described by S. Mantl et al. in Nucl. Instr. and Meth. in Phys. Res., Vol. B 147, p. 29, 1999, and by B. Holländer et al. in Nucl. Instr. and Meth. in Phys. Res., Vol. B 148, p. 200, 2000, hydrogen is implanted at some depth below the SiGe epilayer. In the subsequent annealing steps, micro cavities form which seem to promote the nucleation of dislocation loops. The latter can extend at the interface and act as misfit segments enabling strain relaxation.

[0017] An alternative method has been proposed by J. Kuchenbecker et al. in Thin Solid Films, Vol. 389, p. 146, 2001. In this paper, the Si wafer is exposed to a low-energy hydrogen plasma, and annealed for a short time, before the epitaxial growth of the SiGe layer by MBE. Similar to H-implantation, this process induces cavities below the interface, which again promote relaxation of the SiGe film upon annealing.

[0018] It is regarded as a disadvantage of these approaches, that for growth in one single step, Ge concentrations in the VS appear to be limited to approximately 20%.

[0019] Another approach - which is essentially similar to the previous one - is referred to as post SiGe growth helium ion implantation plus annealing. It differs from the previous approach in that the implanted species is He rather than H. It has, however, been shown to work up to Ge concentrations of 30% (cf. B. Holländer et al., Nucl. Instr. and Meth. in Phys. Res. B 175-177, p. 357,

2001). Transistor data obtained on 95 nm thick $Si_{0.69}Ge_{0.31}$ VS are comparable to those obtained on conventional graded VS (cf. H.-J. Herzog et al., IEEE Electron Device Letters, Vol. 23, p. 485, 2002.

[0020] VS growth by hydrogen and He implantation plus annealing could be used in industrial production, provided that the SiGe layers are grown by a gas phase process rather than by MBE, as in all publications mentioned above.

[0021] As addressed above, several approaches have been suggested and implemented to decrease the thickness of the VS to below ~ 500 nm. While partially successful from a scientific point of view, all these approaches rely for the most part on processes unsuitable for large scale production.

[0022] It is a disadvantage of the known CVD approaches that the growth rate is low. Since a certain minimum thickness of ~100nm of the semiconductor layer (e.g., a SiGe VS) is required, the formation of this layer takes quite some time when using conventional approaches. This is, however, highly unfavorable for industrial mass production.

[0023] It is an object of the present invention to provide a method for making thin, highly relaxed semiconductor layers using processes suitable for large scale production.

[0024] It is an object of the present invention to provide a method for making SiGe layer(s) having a high degree of relaxation.

[0025] It is an object of the present invention to provide heterostructure devices made by such methods.

Summary of the present invention

[0026] The present invention relies on a low-energy plasma enhanced chemical vapor deposition (LEPECVD) process.

[0027] According to the present invention, a method for forming thin (between 100nm and 800nm) highly relaxed semiconductor layers is proposed. It comprises the following steps:

- providing a substrate (e.g., a silicon wafer) in a growth chamber on a substrate carrier,
- maintaining a constant substrate temperature (T_S) of the substrate in a range between 350^{0}C and 500^{0}C,
- establishing a high-density, low-energy plasma in the growth chamber such that the substrate is being exposed to the plasma,
- directing Silane gas (SiH_4) and Germane gas (GeH_4) through the gas inlet into the growth chamber, the flow rates of the Silane gas and the Germane gas being adjusted in order to form said semiconductor layer by means of low-energy plasma enhanced chemical vapor deposition with a growth rate in a range between 1 and 10 nm/s, said semiconductor layer having a Germanium concentration in a range between $0 < x < 50\%$.

[0028] Various advantageous methods are claimed in the dependent claims 2 through 17.

[0029] According to the present invention, heterostructure semiconductor devices are proposed. Such a device comprises a substrate, a $Si_{1-x}Ge_x$ layer with constant concentration x of Ge, and an active region being situated above said $Si_{1-x}Ge_x$ layer. The $Si_{1-x}Ge_x$ layer has a thickness between 100nm and 800nm and a degree of relaxation of at least 75%.

[0030] Various advantageous devices are claimed in the dependent claims 19 through 22.

[0031] In contrast to those processes and approaches described above, the present invention concerns a gas phase process suitable for semiconductor production. None of the other well-known gas phase processes, atmospheric pressure chemical vapor deposition (APCVD), reduced pressure CVD (RPCVD), low pressure CVD (LPCVD), ultra-high vacuum CVD (UHV-CVD), is applicable at

the low substrate temperatures in question, because of their exceedingly low deposition rates (mono-layers per minute or less).

[0032] The fabrication of a VS suitable for n-MODFET or MOSFET production requires, according to the present invention, one single substrate temperature only during the growth plus one subsequent annealing step. This annealing step is optional.

[0033] In the mixed MBE/LEPECVD technology described and claimed below, this annealing step is part of the substrate preparation prior to active layer growth by MBE.

[0034] The fabrication of a thin VS suitable for p-MODFET or MOSFET production requires at most two substrate temperatures during growth.

[0035] It is another advantage of the present invention that the process is fast. The deposition of the thin VS requires less than 5 min for all relevant Ge concentrations and thicknesses. All prior art gas phase processes described above are slower by at least a factor of 10^3. In this comparison only the actual deposition time is counted. Taking into account the time consuming variation of substrate temperatures, the competing processes are even slower.

[0036] The process presented herein is characterized in that a one-step fabrication of a thin SiGe VS is possible for Ge concentrations up to 50 %.

[0037] It is another advantage of the invention presented herein, that the obstacles and disadvantages of known approaches can be circumvented or even avoided. The growth rate was drastically increased thus allowing the inventive process to be used for industrial manufacturing of semiconductor devices. Further advantages become obvious from the detailed description.

Brief descripti n of the drawings

[0038] For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic cross-section of a low-energy plasma enhanced chemical vapor deposition (LEPECVD) system, according to the present invention;

FIG. 2 is a diagram depicting the degree of relaxation as a function of the thickness *t* for a thin layer grown in a one-step LEPECVD, according to the invention, before and after annealing at different temperatures;

FIG. 3 is a diagram depicting the root-mean-square roughness as a function of the thickness *t* for a thin layer grown in a one-step LEPECVD, according to the invention, before and after annealing at different temperatures;

FIG. 4 is a schematic cross-section of a SiGe heterostructure semiconductor device (n-MODFET), according to the present invention;

FIG. 5 is a schematic cross-section of another SiGe heterostructure semiconductor device (p-MODFET), according to the present invention;

FIG. 6 is a schematic cross-section of a device, according to the present, comprising a Silicon-on-Insulator (SOI) substrate.

Detailed Descripti n:

[0039] The present invention relies on low-energy plasma enhanced chemical vapor deposition (LEPECVD). A typical LEPECVD system 20 is depicted in Fig. 1. LEPECVD is based on a low-voltage DC arc discharge between a hot filament 21 in a plasma chamber 22 and the walls of the growth chamber 23 and/or an auxiliary anode 24. A Si substrate 25 on which a thin highly relaxed SiGe semiconductor layer is to be formed in a one-step process is exposed directly to the high-intensity but low-energy plasma. The substrate potential is around – 12 V, for example, in order to exclude any damage of the substrate 25 by high-energy ions. An appropriate bias may be applied to the substrate 25 by means of a bias control unit 31 in order to guarantee this value. It is also possible to use a floating substrate 25 where no bias is applied during deposition which means that the substrate potential is not externally controlled during deposition.

[0040] The LEPECVD is characterized in that the plasma potential is close to 0V. The necessary reactive gases, e.g., Silane (SiH_4) and Germane (GeH_4), are fed through a port 26 and a gas inlet 30 directly into the growth chamber 23, while the argon (Ar) discharge gas is supplied through a port 27 to the plasma chamber 22 attached to the growth chamber 23 and separated from it by a small orifice 28. The high intensity of the plasma leads to very efficient cracking of the precursor gases (e.g., SiH_4, GeH_4), resulting in extraordinarily high growth rates of SiGe films. The growth rates are further enhanced by confining the plasma by a magnetic field generated by coils wrapped around the growth chamber 23. An appropriate voltage is used to drive an alternating current through the filament 21. This current (about 130A in the present embodiment) heats the filament 21 to the desired temperature. In addition, a DC voltage source 32 (about 25V) between the filament 21 and ground is used to generate the arc discharge. In the present system 20, the density of the arc current at or near the substrate 25 is at least 0.2 A/cm^2. Preferably, the density of the arc current is adjusted to be greater than 0.3 A/cm^2.

[0041] Further details of LEPECVD systems are addressed in the above-mentioned PCT patent application WO 98/58099, for example. Details of this PCT patent application are incorporated by means of reference.

[0042] It is an advantage of an LEPECVD system that very high plasma densities can be achieved. According to the present invention, such a high density plasma is used for the growth of a thin semiconductor layer (virtual substrate). The cracking of the reactive gases is very efficient in a high density plasma thus increasing the growth kinetics. Extremely high growth rates of up to 10 nm/s are possible at substrate temperatures T_S between 350^0C and 500^0C. In contrast to conventional chemical vapor deposition (CVD) systems, the growth rate in an LEPECVD system is almost completely independent of the substrate temperature in the given temperature range.

[0043] Furthermore, it has been demonstrated that according to the present invention the SiGe growth rate in an LEPECVD system is almost independent of the concentration of the gas reactants in the growth chamber at a constant total flow, whereas in conventional CVD systems there is a strong dependency between the growth rate and the gas concentrations. It is thus an advantage of the present system, that larger thickness and composition can be more easily controlled.

[0044] Using an LEPECVD system to carry out the inventive process steps, synthetic devices having a thin virtual substrate can be grown at very high growth rates in a range between 1 and 10 nm/s. Typical growth rates in an MBE system are between 0.1 and 0.3 nm/s. The growth rates in a UHV-CVD system are at least another order of magnitude lower at comparable substrate temperatures.

[0045] According to the present invention, a new one-step gas phase process based on LEPECVD is proposed which has the following characteristics:

- low substrate temperatures T_S between 350^0 and 500^0 C;
- the substrate temperature T_S is kept constant during deposition of the entire VS;

- SiGe deposition rates in a range between 1 nm/s and 10 nm/s, and preferably on the order of 2 nm/s;
- SiGe layer thicknesses in a range between 100nm and 800nm.

[0046] Furthermore, during the formation of the virtual substrate the density of the plasma is kept at a high level.

[0047] Subsequent to the forming of the thin semiconductor layer (VS), an optional annealing step may be carried out. The annealing, according to the present invention, is done at moderate temperatures (typically in a range between 600°C and 870°C) before growth of an active layer stack, for instance. Rapid thermal annealing (RTA) is particularly well suited for being used in connection with the present invention.

[0048] According to the present invention, the substrate temperature T_S is not altered during formation of the thin virtual substrate. That is, according to the present invention, the substrate temperature T_S is maintained constant during the formation of the semiconductor layer, which means that the substrate temperature preferably has a maximum fluctuation of ± 5%.

[0049] A method for forming a thin semiconductor layer with a thickness between 100nm and 800nm, in accordance with the present invention, comprises the following steps:

- A substrate (e.g., a silicon wafer) is placed in the growth chamber (23) on a substrate carrier.
- The substrate temperature T_S of the substrate is increased and then maintained at a constant substrate temperature in a range between 350°C and 500°C during the formation of the thin semiconductor layer. Preferably, the substrate temperature T_S is kept in a range between 380°C and 420°C.
- A high-density, low-energy plasma is established in the growth chamber (23) such that the wafer is exposed to the plasma.
- Silane gas (SiH_4) and Germane gas (GeH_4) are directed through the gas inlet 26, 30 into the growth chamber 23. The flow rates of the Silane gas and the Germane gas are adjusted in order to form said thin semiconductor

layer by means of a one-step vapor deposition process with a growth rate in a range between 1 and 10 nm/s. Preferably, the growth rate is in a range between 1.5 nm/s and 4 nm/s. The thin semiconductor layer has a Germanium concentration in a range between $0 < x < 50\%$.

[0050] Contrary to what was to be expected when extrapolating experimental data from known gas phase processes, according to the present invention, low substrate temperatures between 350^0 and 500^0 C, preferably in the range between 380^0C and 420^0C, are very well suited. Not only is the growth rate at these low temperatures high, but also the quality of the layers is much better than expected. It turns out that the process parameters and the one-step process described and claimed herein especially allow thin high-quality non-graded SiGe layers to be grown with a high degree of relaxation R.

[0051] The degree of relaxation R is defined as follows. Designating the lattice parameter of the free standing alloy (that is its bulk lattice parameter) by a_{SiGe}, the Si lattice parameter by a_{Si}, and the measured lattice parameter of the epitaxial alloy parallel to the substrate interface as a_{par}, R is given by $R = (a_{par}-a_{Si})/(a_{SiGe}-a_{Si})$. A layer with a high degree of relaxation is herein referred to as highly relaxed layer. For the purposes of the present specification and claims, a highly relaxed layer is deemed to have a degree of relaxation of at least 75%.

[0052] The method for forming a thin highly relaxed semiconductor layer takes in any case less than 5 minutes, preferably between 1 and 4 minutes. This is another clear distinction over processes known so far.

[0053] Preferably, a <100> or <111> oriented silicon wafer is employed.

[0054] In a advantageous embodiment of the invention, the substrate has a potential of about – 12 Volts and the plasma potential is close to 0 Volt.

[0055] According to another embodiment, a thin silicon buffer layer is formed on the silicon wafer prior to the forming of the thin higly relaxed

semiconductor layer. The thin silicon buffer layer preferably is formed at a substrate temperature T_S in a range between 700°C and 750°C.

[0056] In an optional step, the uppermost part of the silicon wafer is treated by means of a dry-etching or wet-etching step prior to the forming of the thin semiconductor layer.

[0057] In a preferred embodiment, the total reactive gas flow at the gas inlet is kept between 5 sccm and 50 sccm so as to allow a growth rate in a range between 1 and 10 nm/s.

[0058] The relaxation of the thin semiconductor layer is a crucial point that needs to be optimized in order for this thin layer to be suited for use in the manufacturing of semiconductor devices. The process parameters (substrate temperature, ...) for the inventive one-step process and the characteristics of the thin semiconductor layer (Ge concentration, thickness *t*) are intentionally chosen to provide for a degree of relaxation of at least 75% (cf. Fig. 2).

[0059] Fig. 2 shows the degree of relaxation measured by X-ray diffraction of a thin $Si_{0.56}Ge_{0.44}$ VS, as grown by LEPECVD (solid line) as a function of the layer thickness *t* expressed in nm. The other curves show the degree of relaxation after an optional annealing step was carried out. The annealing has been carried out at the following temperatures: 600°C, 700°C, 830°C, 870°C, 955°C, and 970°C. It should be noted that 300 to 500 nm thick films are about 97% relaxed upon annealing to 830°C. Even a 90 nm thick VS has a degree of relaxation of 87% after annealing to this temperature. Furthermore, for films thicker than ~ 300 nm, the final state of relaxation (about 97%) is reached already at an annealing temperature of 700°C. Annealing above 900°C does, however, degrade the thin film and the surface quality.

[0060] The results depicted in Fig. 2 reveal that an optional annealing step may be carried out after completion of the one-step deposition of the thin semiconductor layer. The annealing step preferably is being carried out at a

temperature T_S in a range between 600°C and 870°C. This leads to favorable results as far as the degree of relaxation is concerned.

[0061] The degree of relaxation achieved for the LEPECVD grown thin films described and claimed herein, compares favourably with that of similar films grown by very low temperature MBE (cf. K. Lyutovich et al., Mat. Sci. Eng. Vol. B 89, p. 341, 2002).

[0062] In the following, the surface morphology of inventive thin films is addressed. The surface structure of all thin VS with a Ge concentration below about 50% is characterized by a cross-hatch found also on thick, linearly graded buffer layers. The root mean square (rms) roughness and peak-to-valley height differences of inventive thin films are, however, substantially smaller. In other words, the thin VS are smoother than the conventional VS. This is another advantage of the inventive one-step process.

[0063] The surface roughness of the same thin $Si_{0.56}Ge_{0.44}$ VS samples, as in Fig. 2, has been evaluated by atomic force microscopy (AFM). The results are presented in Fig. 3. The rms values are below 1.5nm for all VS up to a thickness t of 500nm and below 1.8nm for all VS up to a thickness t of 800nm and annealing temperatures < 870°C. This is substantially below the value for a conventional VS graded to the same concentration. The values compare also favourably with those in the literature obtained by MBE on comparable or lower Ge concentrations:

- 1.2nm for 500nm $Si_{0.7}Ge_{0.3}$ (J.H. Li et al., Appl. Phys. Lett., Vol. 71, p. 3132, 1997);
- 1.8nm for 500nm $Si_{0.7}Ge_{0.3}$ (C.S. Peng et al., Appl. Phys. Lett., Vol. 72, p. 3160, 1998)),
- ~ 4.9nm for 500nm $Si_{0.6}Ge_{0.4}$ (T. Ueno et al., Thin Solid. Films, Vol. 369, p. 320, 2000)).

[0064] An even smaller surface roughness can be achieved for VS with a higher Ge content, by using a two-step process in which a thin film semiconductor layer (alloy) with a lower Ge concentration is deposited first using

the inventive one-step process, followed by an alloy layer (second semiconductor layer) with a higher Ge concentration. AFM images have been obtained on a 220nm thick $Si_{0.28}Ge_{0.72}$ buffer layer on top of 150nm of $Si_{0.55}Ge_{0.45}$ both grown at a substrate temperature of 400°C. Here, the cross-hatch is very faint, and the rms roughness amounts to only 0.7 nm. This may be compared with the value of 2.3 nm obtained on a $Si_{0.4}Ge_{0.6}$ buffer in the MBE work of C.S. Peng et al., Appl. Phys. Lett., Vol. 72, p. 3160, 1998.

[0065] It is an advantage of the specific set of process parameters identified above, that the thin semiconductor layer shows a self-relaxation during formation. This allows a thin semiconductor layer to be formed that has a relaxation of more than 75% after completion of the one-step deposition. Furthermore, thin highly relaxed semiconductor layers, according to the present invention, have a surface roughness (rms) of less than 1.8nm and/or a peak-to-valley height difference of less than 5nm.

[0066] According to the present invention, a further step may be carried out after the one-step deposition of the thin semiconductor layer, as addressed above. During this further step a second semiconductor layer is formed having a Germanium concentration in a range between $50 < x < 100\%$. This second semiconductor layer can be formed at a second substrate temperature T_{S2}. Preferably, this second substrate temperature T_{S2} is similar to, or a little bit lower than the substrate temperature T_S used during the one-step deposition of the thin semiconductor layer. Preferably: $T_S-50^0C < T_{S2} \leq T_S$.

[0067] The new process, according to the present invention, can be combined in a mixed technology with others, such as MBE or UHV-CVD, for growth of the active layer stack on top of the thin VS. Alternatively, active layers can be grown on top of the thin VS by LEPECVD itself. The invention is thus also applicable to devices with strained channels.

[0068] The new process can be used in a mixed technology, together with a state of the art deposition process, such as MBE or UHV-CVD, as stated above. A schematic set-up for n-modulation doped field effect transistor (MODFET)

structures is shown in Fig. 4. Please note that the thickness of the various layers are not drawn to scale. The MODFET 50 comprises the following layers. It comprises a Si substrate 51 on which a thin Si buffer 52 is formed. A <001> oriented 1500-3000Ωcm n-type (P) or p-type (B) Si wafer may serve as Si substrate 51. The buffer 52 comprises 20nm Si grown at 750°C at a growth rate of 0.15 nm/s followed by 100nm Si grown at 750°C at a growth rate of 0.72 nm/s. On top of this buffer 52, a thin SiGe VS 53 is formed (thickness of about 500nm). The composition of this VS 53 is: $Si_{0.58}Ge_{0.42}$. The VS 53 is grown at 400°C at a growth rate of 2 nm/s using LEPECVD, according to the present invention. The VS 53 is not graded, i.e. the VS 53 has a constant Ge concentration where the concentration x=0.42. The following steps are now formed using an MBE-based process.

[0069] An active region 59 is situated on the VS 53. It comprises a $Si_{0.6}Ge_{0.4}$ cladding layer 54 followed by a spacer 55 above a δ-doping spike (Sb) (modulation doped layer). A Si channel 56 is situated on top of the spacer 55. The Si channel is about 10 nm thick. On top of the channel 56 there is a spacer 57 followed by a δ-doping spike (Sb) (modulation doped layer) and a $Si_{0.6}Ge_{0.4}$ cladding layer 58. Note that each of the modulation doped layers 55 and 57 only comprise one doping spike. Instead of modulation doped layers with spike, one can also use a thicker layer having a constant dopant concentration.

[0070] Electrical measurements have been performed on van-der-Pauw squares. These measurements show that the electron mobilities obtained for a VS grown by the inventive process can compete with a well established MBE reference which consists of a standard graded buffer as VS. The results with the mixed technology and thin VS fabrication by the inventive process are almost as good as those obtained by using thick conventional VS grown by LEPECVD.

[0071] It must be emphasized that in the mixed technology process described here LEPECVD and MBE steps have been carried out in two separate growth systems, requiring wet chemical cleaning of the VS and oxide desorption in the MBE prior to active layer growth. The oxide desorption in the MBE implies an annealing step at typically 700°C. In a practical realization of the mixed

technology, the two systems (LEPECVD and MBE) would be coupled in order to avoid exposure of the VS to the ambient.

[0072] Yet another embodiment is described in connection with Fig. 5. According to this embodiment, the thin VS and the active layer stack are grown by LEPECVD. The Fig. 5 shows the set-up for a p-MODFET structure where the VS substrate is fabricated by the inventive LEPECVD process, and the active layer stack by the LEPECVD process described in PCT/EP02/09922.

[0073] Please note that the thickness of the various layers are not drawn to scale. The p-MODFET 60 comprises the following layers. It comprises a Si substrate 61 on which a thin Si buffer 62 is formed. A <001> oriented >1000Ωcm n-type (P) or p-type (B) Si wafer may serve as Si substrate 61. The buffer 62 comprises 17nm Si grown at 750^{0}C at a growth rate of 0.1 nm/s followed by 75nm Si grown at 750^{0}C at a growth rate of 0.5 nm/s. On top of this buffer 62, a thin highly relaxed SiGe VS 63.1 is formed (thickness of about 150nm). The composition of this VS 63.1 is: $Si_{0.55}Ge_{0.45}$. The VS 63.1 is grown at 400^{0}C at a growth rate of 2 nm/s using a LEPECVD, according to the present invention. The VS 63.1 is not graded, i.e. the VS 63.1 has a constant Ge concentration where the concentration x=0.45. In a subsequent step a second semiconductor layer 63.2 is formed as follows: thickness 220nm, composition $Si_{0.28}Ge_{0.72}$, LEPECVD deposition at 400^{0}C at a growth rate of 6.3 nm/s followed by a 5 minute annealing step (annealing temperature of about 500^{0}C).

[0074] An active region 70 is formed on top of the layer 63.2. All layers of the active region 70 are formed using LEPECVD. The layer 64 is a $Si_{0.3}Ge_{0.7}$ layer Having a thickness of 31 nm. A Ge channel 65 is formed next. The Ge channel 65 is 10 nm thick. A $Si_{0.3}Ge_{0.7}$ spacer 66 is deposited on the Ge channel 65. The spacer 66 is 15 nm thick. There is a modulation-doped $Si_{0.3}Ge_{0.7}$ layer 67 having two δ-doping spike (B) with 6 nm between. A 31 nm thick $Si_{0.3}Ge_{0.7}$ cladding 68 is formed on the spacer 66. A 3 nm thick $Si_{0.3}Ge_{0.7}$ layer 69.1 with one δ-doping spike (B) is formed next. Finally, a thin Si cap layer 69.2 is formed on the cladding 68. This Si cap layer 69.2 is about 3nm thick.

[0075] The hole mobility and sheet carrier density of such a structure 60 were measured. The resulting mobility of 13'000 cm^2/Vs at 20K compares favourably with the 11'000 cm^2/Vs obtained by state of the art MBE at a comparable hole density (T. Ueno et al., Thin Solid Films, Vol. 369, p. 320, 2000). These results show that high-quality device material can be obtained by using LEPECVD with the new one-step process for VS fabrication and for active layer growth.

[0076] According to the present invention, the thin SiGe semiconductor layer can also be formed in a one-step process on top of a Silicon-on-Insulator (SOI) substrate. SiGe on a SOI substrate is very well suited for very large scale integration (VLSI) of circuits. A respective embodiment 80 is depicted in Fig. 6. The embodiment 80 comprises a Si substrate 71. A buried SiO_2 layer is formed on top of the substrate 71 followed by a thin Si film 73. This thin Si film has a thickness between 50nm and 500nm. A SiGe layer 74 is deposited by LEPECVD at low substrate temperature T_S. The Ge concentration is between 10% and 40%. The thickness of the SiGe layer 74 is chosen such that layer 74 is unrelaxed during deposition. In a subsequent annealing step, the SiGe layer 74 relaxes. The layers 71 through 74 serve as VS. A relaxed SiGe layer 75 is formed on top of this VS. An active layer stack 76 is situated on said SiGe layer 75. The active layer stack 76 may comprise the layers 55 through 58 of Fig. 4, for example.

[0077] As indicated by the above embodiments, the inventive process can be altered in many ways. The embodiments are not meant to limit the scope in any way.

[0078] The inventive concept is well suited for use in transistors, sensors, spectroscopy, quantum computers, solar cells, and other devices/systems. The present invention is particularly well suited to make n- and p-MODFETs as well as n- and p-MOSFETs and other CMOS circuits.